Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (currently amended) A method of forming a buried strap in the fabrication of a deep trench DRAM integrated circuit device comprising:

providing a deep trench into said substrate;

forming a collar on an upper portion of said deep trench;

filling said deep trench and overlying said collar with a silicon layer wherein said silicon layer forms a deep trench capacitor;

recessing said silicon layer below a top surface of said substrate to leave a recess;

etching away a top portion of said collar to leave a collar divot; and

selectively depositing a selective deposition layer into said deep trench and filling said collar divot wherein said selective deposition layer is not deposited outside of said deep trench to form said buried strap in the fabrication of said deep trench DRAM integrated circuit device.

2. (original) The method according to Claim 1 wherein said collar comprises thermally grown or deposited oxide.

3. (original) The method according to Claim 1 wherein said silicon layer comprises amorphous silicon.

4. (original) The method according to Claim 1 wherein said recess has a depth of between about 50 and 200 nm.

5. (original) The method according to Claim 1 wherein said collar divot has a depth of between about 30 and 50 nm.

6. (previously presented) The method according to Claim 1 wherein said selective deposition layer is selected from the group consisting of: a hemispherical grain polysilicon layer, a SiGe layer, a polysilicon layer, and a pseudo-epitaxial silicon layer.

7. (original) The method according to Claim 1 wherein said step of selectively depositing said selective deposition layer comprises forming a hemispherical grain polysilicon layer to a thickness of between about 20 and 100 nm and having a grain size of between about 10 and 50 nm.

8. (previously presented) The method according to Claim 7 before said step of selectively depositing said hemispherical grain polysilicon layer further comprising plasma doping said silicon layer to amorphize a surface of said silicon layer.

9. (previously presented) The method according to Claim 7 wherein said step of selectively depositing said hemispherical grain polysilicon layer comprises in-situ doping of said polysilicon layer.

10. (original) The method according to Claim 1 after said step of selectively depositing said selective deposition layer further comprising doping said selective deposition layer to a concentration of between about 1E18 and 1E21 ions/cm^3.

11. (previously presented) The method according to Claim 10 wherein said doping step is selected from the group consisting of: plasma doping, plasma ion immersion implantation, and gas phase doping.

12. (currently amended) The method according to Claim 1 further comprising:

forming a shallow trench isolation region partially within said deep trench and said buried strap area; and

annealing said substrate whereby dopants from said buried strap diffuse into said substrate to form a buried strap diffusion and wherein said buried strap diffusion connects said deep trench capacitor to a gate electrodes to complete formation of said deep trench DRAM device.

13. (currently amended) A method of forming a buried strap in the fabrication of a deep trench DRAM integrated circuit device comprising:

providing a deep trench into said substrate;

forming a collar on an upper portion of said deep trench;

filling said deep trench and overlying said collar with a silicon layer wherein said silicon layer forms a deep trench capacitor;

recessing said silicon layer below a top surface of said substrate to leave a recess;

etching away a top portion of said collar to leave a collar divot;

selectively depositing a selective deposition layer into said deep trench and filling said collar divot wherein said selective deposition layer is not deposited outside of said deep trench to form said buried strap;

forming a shallow trench isolation region partially within said deep trench and said buried strap area; and

annealing said substrate whereby dopants from said buried strap diffuse into said substrate to form a buried strap diffusion and wherein said buried strap diffusion connects said deep trench capacitor to a gate electrodes to complete formation of said deep trench DRAM device.

14. (previously presented) The method according to Claim 13 wherein said selective deposition layer is selected from the group consisting of: a hemispherical grain polysilicon layer, a SiGe layer, a polysilicon layer, and a pseudo-epitaxial silicon layer.

15. (previously presented) The method according to Claim 13 wherein said step of selectively depositing said layer comprises in-situ doping of said layer.

16. (previously presented) The method according to Claim 13 after said step of selectively depositing said layer further comprising doping said selective deposition layer to a concentration of between about 1E18 and 1E21 ions/cm^3.

17. (previously presented) The method according to Claim 16 wherein said doping step is selected from the group containing: plasma doping, plasma ion immersion implantation, and gas phase doping.

18. (currently amended) A method of forming a buried strap in the fabrication of a deep trench DRAM integrated circuit device comprising:

providing a silicon nitride layer on a substrate;

etching a deep trench through said silicon nitride layer and into said substrate;

forming a collar on an upper portion of said deep trench;

forming a buried plate around a lower portion of said deep trench;

depositing a dielectric layer on sidewalls of said deep trench;

filling said deep trench and overlying said collar with a silicon layer wherein said silicon layer forms a deep trench capacitor;

recessing said silicon layer below a top surface of said substrate to leave a recess;

etching away a top portion of said collar to leave a collar divot;

selectively depositing a layer into said deep trench and filling said collar divot wherein said layer is not deposited outside of said deep trench to form said buried strap; and

doping said selective deposition layer and annealing said substrate whereby dopants in

said buried strap outdiffuse into said substrate to form a buried strap outdiffusion junction in the fabrication of said deep trench DRAM integrated circuit device.

19. (previously presented) The method according to Claim 18 wherein said step of forming said collar comprises:

growing or depositing an oxide layer within said deep trench; and

thermally densifying said oxide layer.

20. (previously presented) The method according to Claim 18 wherein said silicon layer comprises amorphous silicon.

21. (previously presented) The method according to Claim 18 wherein said selective deposition layer is selected from the group consisting of: a hemispherical grain polysilicon layer, a SiGe layer, a polysilicon layer, and a pseudo-epitaxial silicon layer.

22. (previously presented) The method according to Claim 18 wherein said step of doping said selective deposition layer is selected from the group consisting of: in-situ doping, plasma doping, plasma ion immersion implantation, and gas phase doping.

23. (previously presented) The method according to Claim 18 further comprising forming a capping layer overlying said selective deposition layer.

24. (previously presented) The method according to Claim 23 wherein said step of forming said capping layer is selected from the group consisting of: selective oxide deposition and silicon nitride deposition.

25. (previously presented) The method according to Claim 18 further comprising:

forming a shallow trench isolation region partially within said deep trench and said buried strap area; and

forming gate electrodes wherein said buried strap diffusion connects said deep trench capacitor to one of said gate electrodes to complete formation of said deep trench DRAM device.